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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.		
09/905,318	07/13/2001	William C. Altmann	19570-05858	6174		
7:	590 12/14/2005	EXAMINER				
Perkins Coie LLP 101 Jefferson Drive			NATNAEL, PAULOS M			
Menlo Park, CA 94025-1114			ART UNIT	PAPER NUMBER		
			2614			
			DATE MAIL ED: 12/14/2005			

Please find below and/or attached an Office communication concerning this application or proceeding.

			Application No.		Applicant(s)			
Office Action Summary		09/905,318		ALTMANN, WILLIAM C.				
		Examiner		Art Unit				
			Paulos M. Natnael		2614			
The MAIL Period for Reply	ING DATE of this communi	cation appe	ears on the cover sh	eet with the co	orrespondence ad	Idress		
WHICHEVER IS - Extensions of time rr after SIX (6) MONTH - If NO period for reply - Failure to reply within Any reply received b	STATUTORY PERIOD FO E LONGER, FROM THE MAN hay be available under the provisions of 1S from the mailing date of this comming y is specified above, the maximum stan in the set or extended period for reply by the Office later than three months at adjustment. See 37 CFR 1.704(b).	AILING DATE of 37 CFR 1.136 unication. tutory period will will, by statute, c	TE OF THIS COMN 6(a). In no event, however, I apply and will expire SIX (cause the application to bec	MUNICATION may a reply be time (6) MONTHS from toome ABANDONED	ely filed he mailing date of this o (35 U.S.C. § 133).			
Status								
1) Responsiv	ve to communication(s) file	d on 26 See	ntember 2005					
2a)⊠ This action								
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	closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.							
Disposition of Clai	·		,,					
<u></u>		nnlication						
	Claim(s) <u>1-23</u> is/are pending in the application. 4a) Of the above claim(s) is/are withdrawn from consideration.							
	Claim(s) is/are allowed.							
	is/arc allowed. - <u>18,20 and 21</u> is/are reject	ed						
	9 and 22 is/are objected to							
· · · · · · · ·	are subject to restrict		election requiremen	nt				
		don and/or	election requiremen	111.				
Application Papers								
	cation is objected to by the							
10)☐ The drawin	g(s) filed on is/are:	a)☐ accep	oted or b) object	ed to by the E	xaminer.			
Applicant m	nay not request that any objec	tion to the dr	rawing(s) be held in a	abeyance. See	37 CFR 1.85(a).			
Replaceme	nt drawing sheet(s) including	the correctio	n is required if the dr	awing(s) is obje	ected to. See 37 Cl	FR 1.121(d).		
11)☐ The oath o	r declaration is objected to	by the Exa	miner. Note the att	ached Office	Action or form P1	ΓΟ-152.		
Priority under 35 U	.S.C. § 119							
	gment is made of a claim f ☑ Some * c)[☐ None of:	or foreign p	riority under 35 U.S	S.C. § 119(a)-	(d) or (f).			
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Attachment(s)								
1) Notice of Reference	es Cited (PTO-892)		4) Inter	rview Summary (PTO-413)			
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)			Pap	er No(s)/Mail Date				
B) Information Disclos Paper No(s)/Mail D	sure Statement(s) (PTO-1449 or Fate	5)		mal Patent Application (PTO-152)				

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DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claim 23 rejected under 35 U.S.C. 102(e) as being anticipated by MacInnis et al. U.S. Pat No. 6,738,072.

Considering claim 23, MacInnis teaches a graphics display system with anti-flutter filtering and vertical scaling feature. Fig.4 of MacInnis specifically discloses FIFO 100 which receives the video input signal and a video scaler 104 which scales the video signal input to it. (Note that temporarily storing the video signal in the FIFO is, in effect, retiming the video signal, i.e. by delaying the output the system is retiming it). As to using a common clock, MacInnis teaches utilizing a single clock in the integrated circuit so that "cost" for the IC may be "lower" and "less noise or interference" may also be generated by the one clock. See Col. 36, lines 19-28.

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Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

- (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 4. Claims 1-18 are again rejected under 35 U.S.C. 103(a) as being unpatentable over MacInnis et al.

Considering claim 1, the reference of MacInnis et al. (hereinafter MacInnis) teaches anti-flutter filtering and scaling of graphics and video data. As illustrated In Fig.2, MacInnis discloses digital video input, bypass video input, as well as analog video input. The latter two are input to the video decoder, which includes YUV scaler and TBC 72 the output of which is inputted to the multiplexer. The Multiplexer selects either the digitized analog signal output from the video decoder 50 or the digital video input from the preceding stage. (see col. 4, lines 17-58) MacInnis teaches that the video signals may be analog or digital.

As to the next stage, it would have been obvious to the skilled in the art at the time the invention was made to readily recognize that the source of the digital signal, for example, to be the preceding stage, and the receiver or the IC as the current stage, the video scaler 52 would be considered the next stage.

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Considering claim 2, the system of claim 1, wherein said DVS comprises: a retiming FIFO for retiming the received video received from the preceding stage; and a scaling engine for scaling the retimed video data to match the constant resolution, is met by Line Buffer 178 and Scaler Engine 182 Fig.5, respectively. (see also fig.4, FIFO 100 and video scaler 104)

Considering claim 3, the system of claim 1, further comprising a receiver for receiving a signal containing digital video from the preceding stage, is met by MPEG Decoder 160, fig.5;

Considering claims **4 and 5**, MacInnis et al. discloses CLUT interface and high speed I/O bus system. MacInnis et al does not disclose a TMDS or LVDS signaling. However, the Examiner takes Official Notice in that Transition Minimized Differential Signaling (TMDS) and Low-voltage differential signaling (LVDS) are well known signaling methods in the DVI standard, and therefore, it would have been obvious to the skilled in the art to modify the system of MacInnis by providing such signaling capability in order to improve video transmission from the source to the set-top and/or from the set-top box to the television set.

Considering claim **6**, the system of claim 1, wherein said signal contains audio, is met by audio input 34, fig.1;

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Claim 7 is a method claim of claim 1 and, therefore, claim 7 is rejected for the same reasons as in claim 1.

Claim 8 is a method claim of claim 2 and, therefore, claim 8 is rejected for the same reasons as in claim 2

Considering claim **9**, the method of claim 7, wherein said step of scaling further comprises the step of superimposing an on-screen display (OSD) message, is met by Fig.31 where an embodiment is illustrated which is a flutter filtering and graphics scaling circuit.

Regarding claim 10, see rejection of claim 4.

Regarding claim 11, see rejection of claim 5.

Regarding claim 12, see rejection of claim 6.

Regarding claim 13, see rejection of claim 1.

Regarding claim 14, see rejection of claim 2.

Regarding claim 15, see rejection of claim 4.

Regarding claim 16, see rejection of claim 5.

Regarding claim 17, see rejection of claim 1;

Regarding claim 18, see rejection of claim 2;

As to claims 20 and 21, see rejection of claims 1 and 7.

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Response to Arguments

5. Applicant's arguments filed 12/9/04 have been fully considered but they are not persuasive.

Applicant argues that in MacInnis Chip, incoming digital video signals are not reclocked as they do not pass through the time base corrector 72 and the re-clocking does not take place within the scaler. However, examiner submits that MacInnis teaches a YUV scaler within the Line locked SRC in the video decoder (fig.18) and that the time base corrector 72 ...corrects digitized analog video in the time domain to reduce or prevent jitter. (col. 4, lines 44-46) In other words, the video signal which is a digital signal at this stage is scaled by the YUV scaler and timebase-corrected by TBC 72 within the video decoder. Thus, the claimed scaling and constant-frequency clocking are met by the MacInnis reference.

Allowable Subject Matter

6. Claims **19,22** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Liu et al., U.S. 6,771,714 teaches a timing recovery using the pilot signal in High definition TV, wherein the digital mixer 18 scales the signal using the oscillator loops.

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paulos M. Natnael whose telephone number is (571) 272-7354. The examiner can normally be reached on 10:00am - 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Miller can be reached on (571)272-7353. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

Paulos M. Natnael Primary Examiner Art Unit 2614

PMN December 9, 2005